Amendments to the Claims

Claims 1-23 are pending in the application. Claims 1 and 20 have been amended.

Listing of Claims:

1. (Currently Amended) An integrated circuit comprising:

a two-dimensional pyramid filter architecture of an order 2N-1 to receive input signals, where N is a positive integer greater than two;

a summer circuit;

~~one-dimensional pyramid filters of order 2N-1;~~

~~two-dimensional pyramid filters of order [2(N-1) – 1];~~

said two dimensional pyramid filter architecture of order 2N-1, in operation, capable of producing, on respective clock cycles, at least the following:

pyramid filtered output signals corresponding to output signals produced by two one-dimensional pyramid filters of order 2N-1; and

pyramid filtered output signals corresponding to output signals produced either by four two-dimensional pyramid filters or one two-dimensional pyramid filter of order [2(N-1) – 1] ~~using signal sample matrices of order [2(N-1)-1]~~;

wherein the respective output signals in said two dimensional pyramid filter architecture are summed by the summer circuit on respective clock cycles of said two dimensional pyramid filter architecture.

2. (Original) The integrated circuit of claim 1, wherein N is three; and

wherein said two dimensional pyramid filter architecture of order five, in operation, capable of producing, on respective clock cycles, the pyramid filtered output signals corresponding to output signals produced either by four two-dimensional pyramid filter or one two-dimensional pyramid of order three using four signal sample

matrices $P_{i-1,j-1}^{3x3}, P_{i-1,j+1}^{3x3}, P_{i+1,j-1}^{3x3}, P_{i+1,j+1}^{3x3}$, the pyramid filtered output signals being produced by a plurality of one-dimensional pyramid filters.

3. (Original) The integrated circuit of claim 2, wherein said one-dimensional pyramid filters comprise a sequence of scalable cascaded multiplerless operational units, each of said operational units capable of producing a different order pyramid filtered output signal sample stream.

4. (Original) The integrated circuit of claim 2, wherein said one-dimensional pyramid filters comprise other than one-dimensional multiplierless pyramid filters.

5. (Original) The integrated circuit of claim 2, wherein said two dimensional pyramid filter architecture of order five, in operation, capable of producing, on respective clock cycles, the pyramid filtered output signals corresponding to output signals produced either by four two-dimensional pyramid filters or one two-dimensional pyramid of order three using four signal sample matrices $P_{i-1,j-1}^{3x3}, P_{i-1,j+1}^{3x3}, P_{i+1,j-1}^{3x3}, P_{i+1,j+1}^{3x3}$, the pyramid filtered output signals produced by a plurality of one-dimensional pyramid filters being produced by eight one-dimensional pyramid filters of order three.

6. (Original) The integrated circuit of claim 5, wherein, of the eight one-dimensional pyramid filters of order three, four are applied row-wise and four are applied column-wise.

7. (Original) The integrated circuit of claim 5, wherein said two dimensional pyramid filter architecture of order five, in operation, capable of producing, on respective clock cycles, the pyramid filtered output signals corresponding to output signals produced by four two-

dimensional pyramid filters of order three, the pyramid filtered output signals produced by a plurality of one-dimensional pyramid filters being produced by eight one-dimensional multiplierless pyramid filters of order three.

8. (Original) The integrated circuit of claim 7, wherein, of the eight one-dimensional pyramid filters of order three, four are applied row-wise and four are applied column-wise.

9. (Original) The integrated circuit of claim 2, wherein said two dimensional pyramid filter architecture of order five, in operation, capable of producing, on respective clock cycles, the pyramid filtered output signals corresponding to output signals produced by four two-dimensional pyramid filters of order three, the pyramid filtered output signals produced by a plurality of one-dimensional pyramid filters being produced by other than one-dimensional multiplierless pyramid filters.

B1

10. (Original) The integrated circuit of claim 1, wherein N is three;

said two dimensional pyramid filter architecture of order five, in operation, being capable of producing, on respective clock cycles, at least the following:

output signals produced by four two-dimensional pyramid filters of order three.

11. (Original) The integrated circuit of claim 1, wherein said two dimensional pyramid filter architecture of order five, in operation, capable of producing, on respective clock cycles, the pyramid filtered output signals corresponding to output signals produced by four two-dimensional pyramid filters of order three, the pyramid filtered output signals being produced by two-dimensional pyramid filters other than four two-dimensional pyramid filters.

12. (Original) A method of filtering an image using a two-dimensional pyramid filter architecture of order 2N-1, where N is a positive integer greater than two, said method comprising:

summing, on respective clock cycles of said two dimensional pyramid filter architecture, the following:

pyramid filtered output signals corresponding to output signals produced by two one-dimensional pyramid filters of order 2N-1; and

pyramid filtered output signals corresponding to output signals produced either by four two-dimensional pyramid filters or one two-dimensional pyramid filter of order [2(N-1) – 1] using signal sample matrices of order [2(N-1)-1].

13. (Original) The method of claim 12, wherein N is three;

pyramid filtered output signals corresponding to output signals produced either by four two-dimensional pyramid filters or one two-dimensional pyramid filter of order [2(N-1) – 1] using signal sample matrices of order [2(N-1)-1] comprising output signals produced by four two-dimensional pyramid filters of order three.

14. (Original) The method of claim 12, wherein N is three; and

wherein the pyramid filtered output signals corresponding to output signals produced either by four two-dimensional pyramid filters or one two-dimensional pyramid of order three using four signal sample matrices $P^{3x3}_{i-1,j-1}, P^{3x3}_{i-1,j+1}, P^{3x3}_{i+1,j-1}, P^{3x3}_{i+1,j+1}$, comprise pyramid filtered output signals produced by a plurality of one-dimensional pyramid filters.

15. (Original) The method of claim 14, wherein said one-dimensional pyramid filters comprise a sequence of scalable cascaded multiplerless operational units, each of said operational units capable of producing a different order pyramid filtered output signal sample stream.

16. (Original) An article comprising: a storage medium, said storage medium having stored thereon instructions, that, when executed result in filtering an image using a two-dimensional pyramid filter architecture of order 2N-1, where N is a positive integer greater than two, by:

summing, on respective clock cycles of said two dimensional pyramid filter architecture, the following:

pyramid filtered output signals corresponding to output signals produced by two one-dimensional pyramid filters of order 2N-1; and

pyramid filtered output signals corresponding to output signals produced either by four two-dimensional pyramid filters or one two-dimensional pyramid filter of order [2(N-1) – 1] using signal sample matrices of order [2(N-1)-1].

17. (Original) The article of claim 16, wherein N is three;

pyramid filtered output signals corresponding to output signals produced either by four two-dimensional pyramid filters or one two-dimensional pyramid filter of order [2(N-1) – 1] using signal sample matrices of order [2(N-1)-1] comprising output signals produced by four two-dimensional pyramid filters of order three.

18. (Original) The article of claim 16, wherein N is three; and

wherein the pyramid filtered output signals corresponding to output signals produced either by four two-dimensional pyramid filters or one two-dimensional pyramid of order three using four signal sample matrices $P^{3x3}_{i-1,j-1}, P^{3x3}_{i-1,j+1}, P^{3x3}_{i+1,j-1}, P^{3x3}_{i+1,j+1}$, comprise pyramid filtered output signals produced by a plurality of one-dimensional pyramid filters.

19. (Original) The article of claim 18, wherein said one-dimensional pyramid filters comprise a sequence of scalable cascaded multiplerless operational units, each of said

operational units capable of producing a different order pyramid filtered output signal sample stream.

20. (Currently Amended) An image processing system comprising:

an image processing unit to filter scanned color images;

a summer circuit;

one-dimensional pyramid filters of order 2N-1;

two-dimensional pyramid filter of order [2(N-1) – 1];

said image processing unit including at least one two-dimensional pyramid filter architecture;

said at least one two-dimensional pyramid filter architecture comprising:

a two-dimensional pyramid filter architecture of an order 2N-1, where N is a positive integer greater than two;

said two dimensional pyramid filter architecture of order 2N-1, in operation, capable of producing, on respective clock cycles, at least the following:

pyramid filtered output signals corresponding to output signals produced by two one-dimensional pyramid filters of order 2N-1; and

pyramid filtered output signals corresponding to output signals produced either by four two-dimensional pyramid filters or one two-dimensional pyramid filter of order [2(N-1) – 1] using ~~signal sample matrices of order [2(N-1)-1]~~;

wherein the respective output signals in said two dimensional pyramid filter architecture are summed by the summer circuit on respective clock cycles of said two dimensional pyramid filter architecture.

21. (Original) The system of claim 20, wherein N is three;

pyramid filtered output signals corresponding to output signals produced either by four two-dimensional pyramid filters or one two-dimensional pyramid filter of order [2(N-1) – 1] using

signal sample matrices of order [2(N-1)-1] comprising output signals produced by four two-dimensional pyramid filters of order three.

22. (Original) The system of claim 20, wherein N is three; and

wherein the pyramid filtered output signals corresponding to output signals produced either by four two-dimensional pyramid filters or one two-dimensional pyramid of order three using four signal sample matrices $P^{3x3}_{i-1,j-1}, P^{3x3}_{i-1,j+1}, P^{3x3}_{i+1,j-1}, P^{3x3}_{i+1,j+1}$, comprise pyramid filtered output signals produced by a plurality of one-dimensional pyramid filters.

23. (Original) The system of claim 22, wherein said one-dimensional pyramid filters comprise a sequence of scalable cascaded multiplierless operational units, each of said operational units capable of producing a different order pyramid filtered output signal sample stream.